

Patent Application For: SINGLE-POLY 2-TRANSISTOR BASED FUSE ELEMENT

Inventor: Chandrasekharan Kothandaraman, et al.

Reference No. 2002 P 03440 US

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(Replacement Sheet)

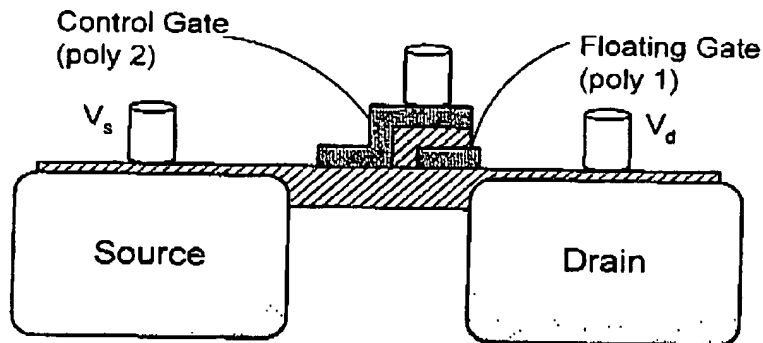


Figure 1



Figure 1A

SG EE	Erase	Program	Read
SG Wordline (WL)	-17 V (-12 V)	V_t	V_{ref}
Bitline (BL)	V_{ss} (5V)	12 V	V_{dd}
Source Line (SR)	V_{ss}	V_{ss}	V_{ss}

Figure 1B

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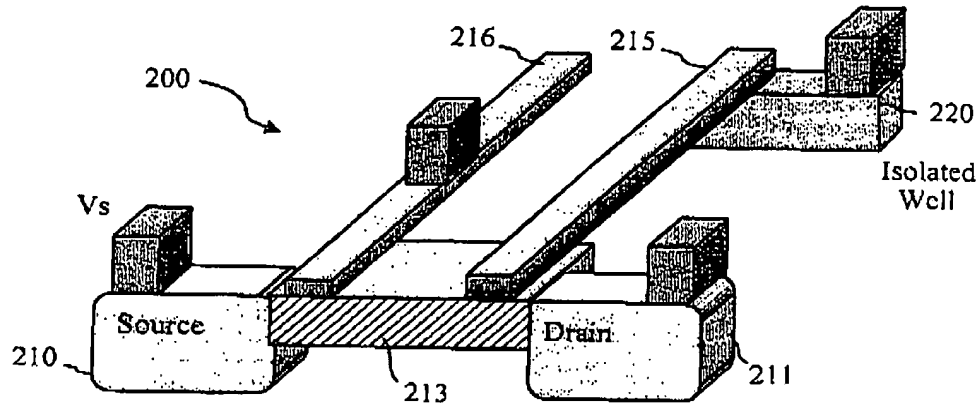


Figure 2A

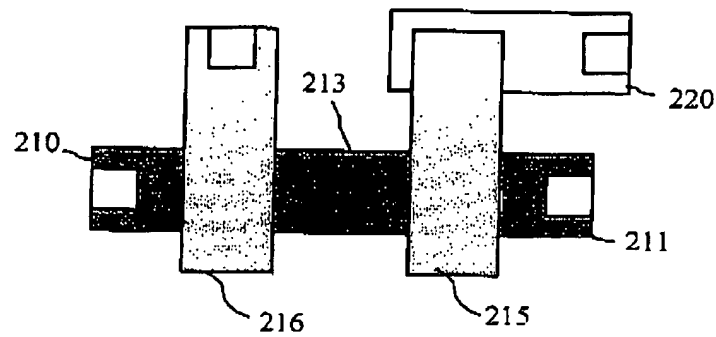


Figure 2B

Parent Application For: SINGLE-POLY 2-TRANSISTOR BASED FUSE ELEMENT

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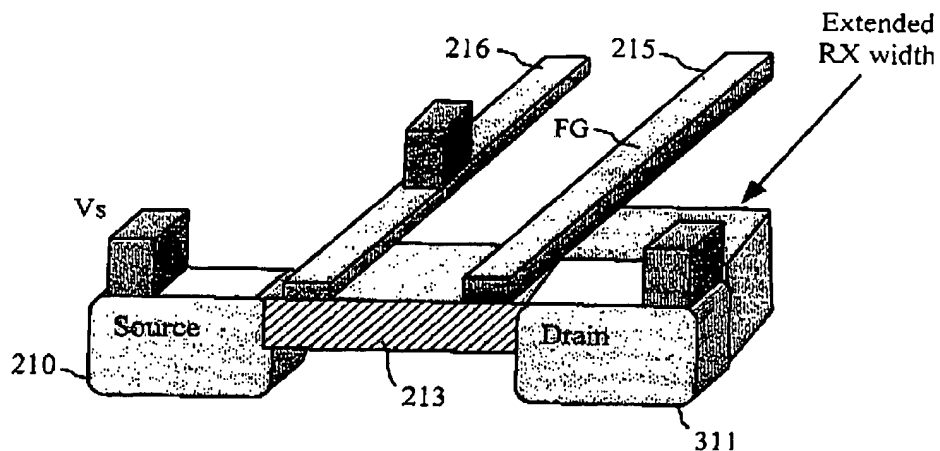


Figure 3A

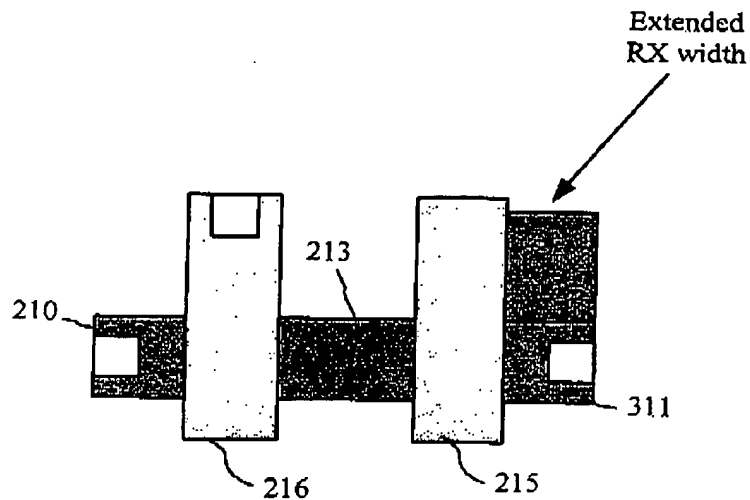


Figure 3B

Patent Application For: SINGLE-POLY 2-TRANSISTOR BASED FUSE ELEMENT

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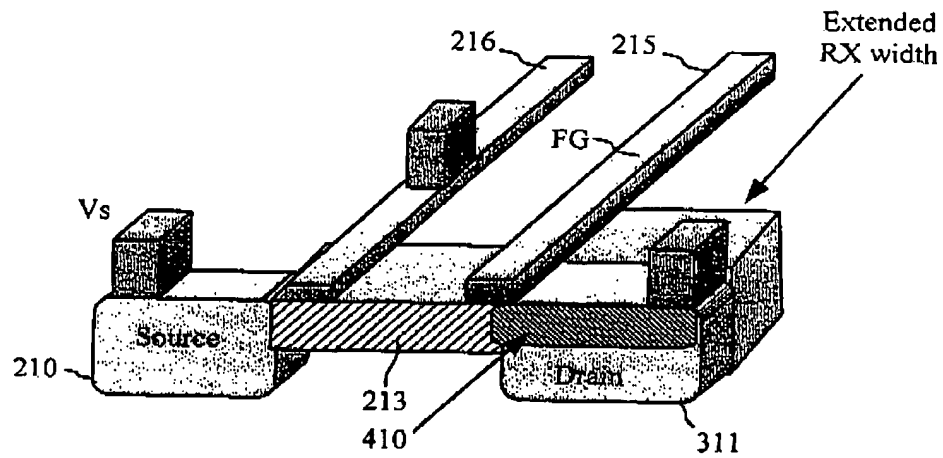


Figure 4A

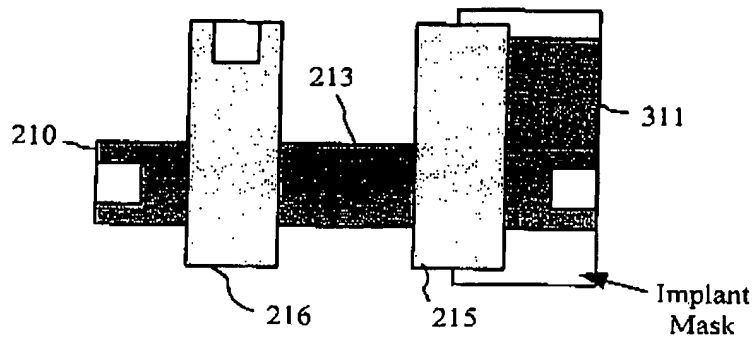


Figure 4B

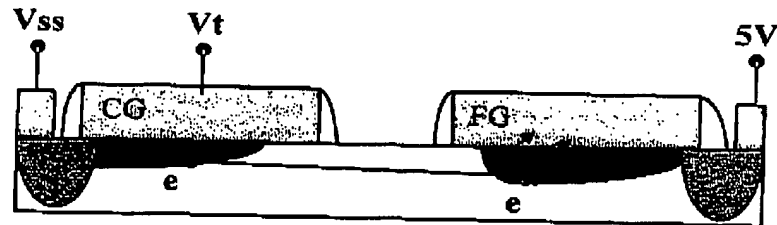
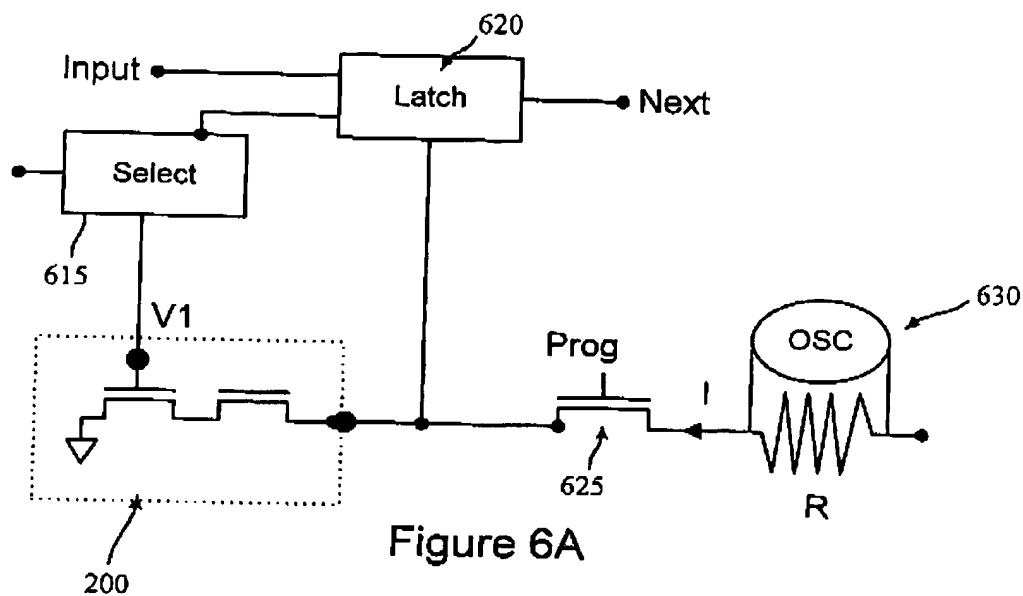


Figure 5A

NVM Fuse	Erase	Program	Read
Selected Wordline	-5 V	V_t	V_{ref}
(BL) (+ iso-well	5 V	5 V	V_{dd}
Source	V_{ss}	V_{ss}	V_{ss}

Figure 5B



NVM fuse	Erase	Program	Read
Select (WL)	-5 V	V _t	V _{ref}
Latch BL (Prog FET)	5V	5 V (on)	V _{dd} (off)
Source	V _{ss}	V _{ss}	V _{ss}

Figure 6B

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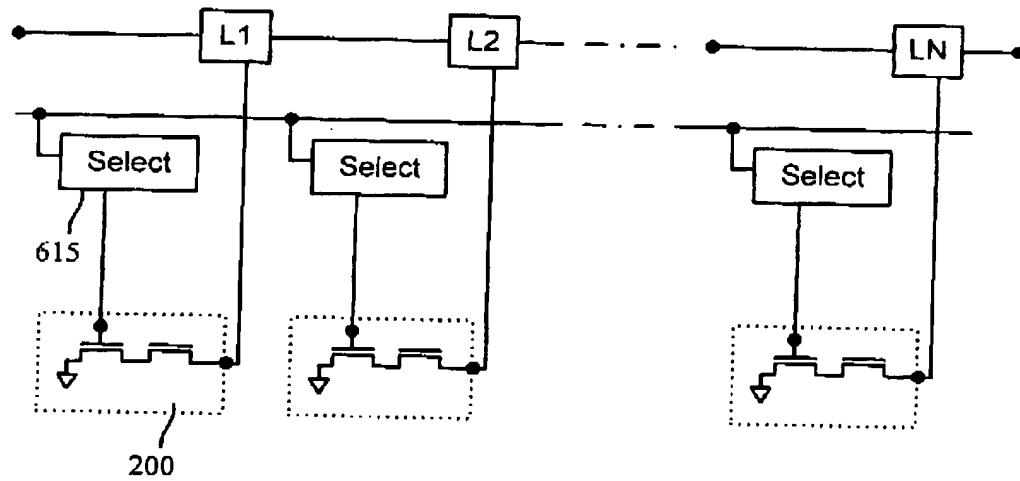


Figure 7A

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